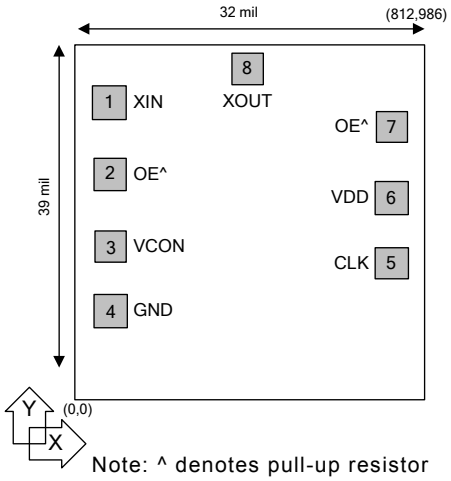
Low Phase Noise VCXO (36MHz to 130MHz)

FEATURES

- VCXO output for the 36MHz to 130MHz range
- Low phase noise (-148 dBc @ 10kHz offset at 77.76MHz).
- CMOS output with OE tri-state control.
- 36 to 130MHz fundamental crystal input.
- Integrated high linearity variable capacitors.
- 8mA drive capability at TTL output.
- +/- 150 ppm pull range, max 5% linearity.
- Low jitter (RMS): 2.5ps period jitter.
- Single 2.5V ±10% or 3.3V ±10 power supply.
- Operating temperature range from -40°C to +85°C
- Available in Die or Wafer form.

PIN AND PAD CONFIGURATION



Note: ^ denotes pull-up resistor

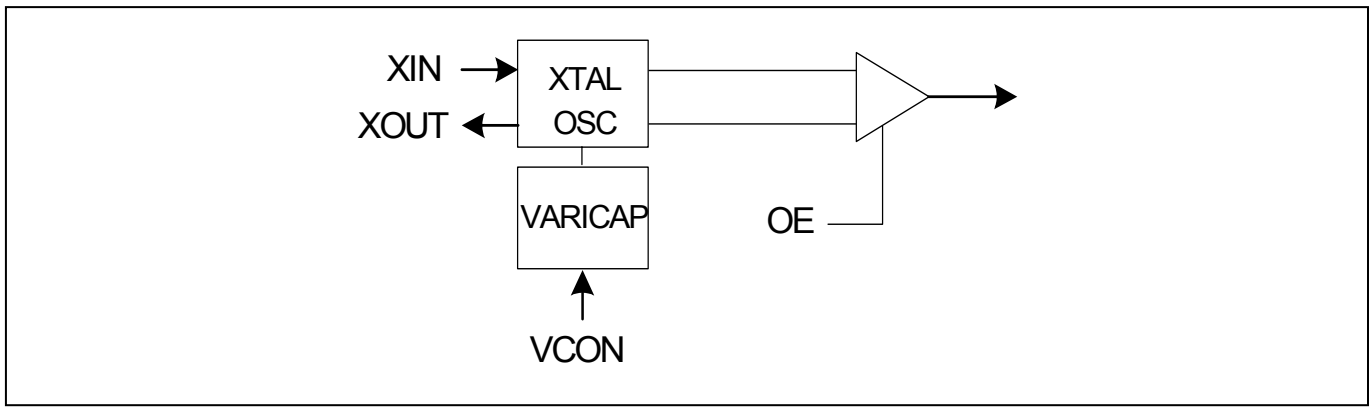
DESCRIPTION

The PLL500-37 is a low cost, high performance and low phase noise VCXO for the 36 to 130MHz range, providing less than -148dBc at 10kHz offset at 77.76MHz. The very low jitter (2.5 ps RMS period jitter) makes this chip ideal for applications requiring voltage controlled frequency sources. Input crystal can range from 36 to 130MHz (fundamental resonant mode).

DIE SPECIFICATIONS

Name	Value
Size	39 x 32 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	12 mil

BLOCK DIAGRAM



PAD ASSIGNMENT AND DESCRIPTION

Name	Pad #	Die Pad Position		Type	Description
		X (μm)	Y (μm)		
XIN	1	94.2	768.6	I	Crystal input pin.
OE	2	94.2	605.0	P	Output Enable input pin. Disables the output when low. Internal pull-up enables output by default if pin is not connected to low. Use only one OE signal.
	7	715.5	626.7		
VCON	3	94.2	331.7	I	Frequency control voltage input pin.
GND	4	94.2	140.4	P	Ground pin.
CLK	5	715.5	203.9	O	Output clock pin.
VDD	6	715.5	455.7	P	VDD power supply pin.
XOUT	8	477.0	888.8	O	Crystal output pin.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			36		130	MHz
Output Clock Rise/Fall Time		0.8V ~ 2.0V with 10 pF load		1.15		ns
		0.3V ~ 3.0V with 15 pF load		3.7		
Output Clock Duty Cycle		Measured @ 1.4V	45	50	55	%
Short Circuit Current				±50		mA

3. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	F_{XIN} = 77.76MHz Output load of 15pF		7.2	9	mA
Allowable output load capacitance	C_L (Output)	Standard drive up to 100MHz			15	pF
Operating Voltage	V_{DD}		2.25		3.63	V
Output Low Voltage at CMOS level	V_{OLC}	I_{OL} = +4mA			0.4	V
Output High Voltage at CMOS level	V_{OHC}	I_{OH} = -4mA	V_{DD} – 0.4			V
Output drive current		For V_{OL}<0.4V or V_{OH}>2.4V	8			mA
Short Circuit Current				±50		mA
VCXO Control Voltage	VCON		0		V_{DD}	V

4. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		F_{XIN} = 36 – 130MHz; XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		300		ppm
CLK output pullability		VCON=1.65V, ±1.65V	±150			ppm
VCXO Tuning Characteristic				100		ppm/V
Pull range linearity					5	%
Power Supply Rejection	PWSRR	Frequency change with VDD varied +/- 10%	-1		+1	ppm
VCON pin input impedance			2000			kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	45			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

5. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}		36		130	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$	VCON = 1.65V		5.0		pF
Maximum Sustainable Drive Level					200	µW
Operating Drive Level				50		µW
C0/C1					250	-
ESR	R_S	C0 ≤ 2.0pF, F_{XIN} up to 85MHz C0 ≤ 2.5pF, F_{XIN} up to 80MHz C0 ≤ 3.0pF, F_{XIN} up to 75MHz			30	Ω
		C0 ≤ 2.0pF, F_{XIN} up to 95MHz C0 ≤ 2.5pF, F_{XIN} up to 90MHz C0 ≤ 3.0pF, F_{XIN} up to 85MHz			25	Ω
		C0 ≤ 2.0pF, F_{XIN} up to 110MHz C0 ≤ 2.5pF, F_{XIN} up to 105MHz C0 ≤ 3.0pF, F_{XIN} up to 100MHz			20	Ω
		C0 ≤ 2.0pF, F_{XIN} up to 130MHz C0 ≤ 2.5pF, F_{XIN} up to 120MHz C0 ≤ 3.0pF, F_{XIN} up to 115MHz			15	Ω

Note: The crystal must be such that it oscillates (parallel resonant) at nominal frequency when presented a C Load as specified above.
If the crystal requires more load to be at nominal frequency, the additional load must be added externally.
This however may reduce the pull range and oscillator gain.

6. Jitter and Phase Noise Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	With capacitive decoupling between VDD and GND.		2.5		ps
Phase Noise relative to carrier	77.76MHz @10Hz offset		-80		dBc/Hz
Phase Noise relative to carrier	77.76MHz @100Hz offset		-110		dBc/Hz
Phase Noise relative to carrier	77.76MHz @1kHz offset		-134		dBc/Hz
Phase Noise relative to carrier	77.76MHz @10kHz offset		-148		dBc/Hz
Phase Noise relative to carrier	77.76MHz @100kHz offset		-150		dBc/Hz
Phase Noise relative to carrier	77.76MHz @1MHz offset		-152		dBc/Hz

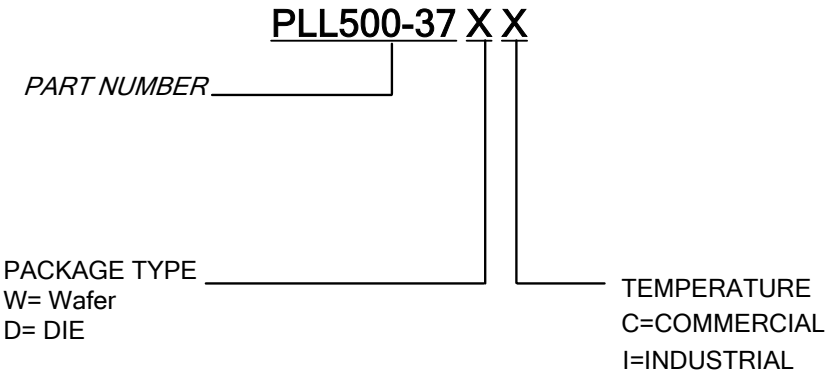
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Part / Order Number	Marking	Package Option
PLL500-37WC	P500-37WC	Wafer
PLL500-37DC	P500-37DC	Die (Waffle Pack)